UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,150	08/02/2001	Jin Chuan Bai	MM4460	7226

7590 11/19/2003

ANDERSON KILL & OLICK P.C.
1251 AVENUE OF THE AMERICAS
NEW YORK, NY 10020-1182

EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/921,150	BAI, JIN CHUAN	
	Examiner	Art Unit	
	David A. Zarneke	2827	

-- The MAILING DATE of this c mmunication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-3 and 5-8 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's first argument is that Booth, Cook and/or Lai all fail to teach screen printing a plurality of conductive elements in direct alignment with the bond pads of a substrate.

The examiner asserts that Booth teaches mask screening (3, 20+) a plurality of conductive elements (4) in direct alignment with the bond pads (8) of a substrate (Figure 6). It is further asserted that mask screening and screen printing are the same thing. Any skilled artisan working the art of printing knows that these are equivalent terms. The examiner will cite proof of this in the rejection below and will include multiple other references as art cited but not relied upon.

Regarding the direct alignment of the conductive features over the bond pads is obviously taught by Booth in Figure 6. It is readily apparent that the conductive features (4) are formed directly over and in alignment with the bond pads (8).

The second argument presented is that the admitted prior art teaches the underfilling of the gap between the chip and the substrate, which is contrary to the present invention.

The examiner takes the position that the references are being attacked individually and not being considered in combination with each other, as in the rejection.

The admitted prior art is relied upon to teach that the encapsulation of a chip mounted on a substrate and the placement of solder balls on the opposite side of the substrate from the chip are conventional to the art. Any and every artisan skilled in the art of semiconductor packaging knows that encapsulation and solder ball placement are the next logical steps in the manufacture of a package.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In no way is this hindsight or contrary to the teachings of Booth. These are the next logical steps in the completion of the packaging of the structure of Booth. Just because Booth does not teach the finishing steps does not make it hindsight or contrary to the teachings of Booth to perform further steps.

Thirdly, applicant argues that Cook teaches the underfilling of the gap between the chip and the substrate and therefore is contrary to the teachings of the present invention.

Again, the examiner takes the position that the references are being attacked individually and not being considered in combination with each other, as in the rejection.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208

USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Cook is relied upon as teaching that the formation of an encapsulant around a chip without fully enclosing chip is known in the art of semiconductor packaging. Any and every artisan skilled in the art of semiconductor packaging knows that an encapsulant can be formed such that the outside surface of the encapsulated chip is exposed to the atmosphere, as in claim 7.

The new rejections of the claims taking into account the claim amendments being newly presented will now be stated.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, US Patent 5,543,585, in view of Applicant's admitted prior art and Takeuchi et al., US Patent Application Publication 2001/0039891.

Booth teaches a direct chip attachment process comprising:

1) preparing a substrate (1) having a first surface and a second surface, wherein at least one chip-mounting area is formed on the first surface with the first surface having a first plurality of bond pads (8) electrically connected to the substrate;

2) screen printing [mask screening] (3, 20+) a plurality of conductive elements (4) on the chip-mounting area of the substrate in direct alignment over each of said first plurality of bond pads (Figure 6), wherein the conductive elements are electrically connected to the substrate and each formed with a flat end;

3) forming a first encapsulant (2) by a mask screening (3, 20-21), which is a type of printing process, on the chip-mounting area of the substrate for encapsulating the conductive elements, wherein the first encapsulant formed by printing is adapted to have a top surface thereof formed in coplanar alignment with the flat ends of the conductive elements to thereby form a common coplanar surface, and the ends of the conductive elements are exposed to the outside of the first encapsulant (Figure 9); and

4) preparing at least one semiconductor chip (6) having a second plurality of bond pads (Figure 14) formed on a surface thereof and mounting the semiconductor chip on the top surface of the first encapsulant in a manner that the second bond pads are electrically connected to the exposed ends of the conductive elements respectively and with the surface of the semiconductor chip closely attached to the coplanar surface formed by the first encapsulant and conductive elements free of any gap between the semiconductor chip and the coplanar surface (Figures 5-9 & 14).

Booth fails to teach the steps 5 and 6, namely the encapsulating of the chip and the implanting of solder balls onto the opposite side of the substrate.

Applicants admitted prior art teaches that it is well known in the art to encapsulate a chip and to implant solder balls to the opposite side of the substrate (specification, page 1, 3rd paragraph).

It would have been obvious to one of ordinary skill in the art to use the chip encapsulation and solder ball implantation of Applicant's admitted prior art in the invention of Booth because these are conventional step used in the packaging of a chip.

The use of conventional materials to perform there known functions in a conventional process is obvious. *In re Raner* 134 USPQ 343 (CCPA 1962).

Takeuchi is cited as support for the assertion that mask screening is the same as screen printing. The abstract teaches that a screen mask is used for screen printing. Further, the specification is replete with instances of talking about a mask or screen mask used in screen printing.

Regarding claim 2, Booth teaches the conductive elements as being conductive bumps (3, 1).

With respect to claim 3, while Booth teaches a conductive adhesive as the conductive element (3, 21+), tin, lead, or a tin/lead alloy conductive element is an equivalent type of conductive element that is commonly used in the art.

While Booth lists a few undesirable attributes of solder alloys, Booth states that solder alloys are pervasively used to interconnect components to carriers (1, 22+).

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution. Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

As to claim 5, Booth teaches the use of conductive metal contacts (8), aka bond pads, electrically connected to chip sites on the surface of the substrate (2, 52+).

Regarding claim 6, Booth teaches the 2nd surface of the chip as having no bond pads (Figure 14).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, US Patent 5,543,585, in view of Applicant's admitted prior art and Takeuchi et al., US Patent Application Publication 2001/0039891, as applied to claim 1 above, and further in view of Cook, US Patent 6,331,446.

Booth and Applicant's admitted prior art both fail to teach the 2nd encapsulant as exposing the outside surface of the chip, which has no bond pads.

Cook teaches a process of underfilling a C4 IC package comprising a 2nd encapsulant that forms a fillet around the edges of the chip without encapsulating the outer surface of the chip (Figure 3).

It would have been obvious to one of ordinary skill in the art to use the fillet of Cook in the combined invention of Booth and Applicant's admitted prior art because Cook teaches that the fillet seals the edges of the chip and the underfill such that moisture migration is inhibited and chip and/or underfill cracking is prevented (2, 56+).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, US Patent 5,543,585, in view of Applicant's admitted prior art and Takeuchi et al., US Patent Application Publication 2001/0039891, as applied to claim 1 above, and further in view of Lai, US Patent 6,323,066.

Booth and Applicant's admitted prior art both fail to teach the use of a heat sink that is encapsulated by the 2nd encapsulant.

Lai teaches a heat-dissipating structure comprising attaching a chip to a substrate, attaching a heat sink to the substrate and over the chip, and then encapsulating the heat sink and the chip (Figure 6).

It would have been obvious to one of ordinary skill in the art to use the heat sink of Lai in the combined invention of Booth and Applicant's admitted prior art because Lai teaches that this type of heat sink arrangement prevents resin flow during the molding process and also prevents the heat sink from causing a thermal compressive stress in the chip during cooling (2, 30+).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Application Publications 2002/0192529 [0045] (Nakamura et al.), 2002/0092825 [0058] (Schneider et al.), and 2001/046553 [0041] (Umemoto et al.) all teach the equivalence of mask screening with screen printing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-F 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703)-308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703)-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-6789.

David A. Zarneke
Primary Examiner
November 15, 2003